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LARGE SIGNAL PERIODIC TIME-DOMAIN SIMULATION

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SUMMARY

A novel algorithm has been implemented within our new semiconductor device simulation program TESSA that allows large signal periodic time-domain simulation to be performed by integrating over just one period of the excitation. Conventionally the need to integrate out initial transients, over many cycles, had effectively made such simulations impracticable. The algorithm can also be implemented in the field of circuit simulation so a combined large signal circuit/device simulation package is now a practical possibility.

INTRODUCTION

Large signal periodic effects are an important class of problem that have, in the past, not been amenable to direct time-domain simulation. Examples of such effects in semiconductor devices are: distortion and duty cycle electrothermal interactions. The fact that the system being modelled may have time constants that are large compared to the fundamental excitation frequency has meant that many cycles must be integrated to avoid transient effects and achieve a true periodic steady state (PSS). Such simulations have therefore been prohibitively expensive in computer time.

In this paper we will be concentrating on modelling distortion effects in semiconductor devices. Conventionally the approach has been to use a parameterized compact circuit model of the device and to employ either frequency domain Volterra series expansion techniques or the harmonic balance approach.[1] However, the need for a circuit model of the device presents a number of problems, particularly from the point of view of device design and optimization. The major problem is that any compact circuit model must degrade the quality of the simulation due to a loss of 'physics'. Also whilst it may be possible to achieve a good circuit representation of an existing device, a lack of direct correspondence between circuit model elements and the physical structure of the device means that the effect of device structural changes are not easily predictable.

We have developed and implemented a novel algorithm based on a space-time formulation of the semiconductor device equations that enables large signal periodic effects to be simulated in the time domain by integrating the governing equations over just one cycle of the fundamental excitation frequency.[2] In this paper details of the algorithm will be presented together with relevant aspects of its implementation within our semiconductor device simulation program TESSA[3] (Thermal and Electronic Semiconductor SimulAtor). Example problems of, single signal source, harmonic distortion in diodes and transistors will be solved and the extension of the algorithm into the realm of circuit simulation will be discussed.

SPACE-TIME FORMULATION OF SEMICONDUCTOR DEVICE EQUATIONS

The basic transient equations for the simulation of semiconductor devices, neglecting thermal effects for simplicity, consist of three continuity equations for the electric field (E), electron current (J_n) and hole current (J_p) together with subsidiary equations relating the field and currents to the fundamental variables electric potential (ψ), electron concentration (n) and hole concentration (p). Conventionally these equations are expressed as:

$$\nabla\cdot\vec{\mathbf{E}} = \frac{q}{\epsilon}(D+p-n) \tag{1}$$

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$$\nabla\cdot\vec{\mathbf{J}}_n - \frac{\partial n}{\partial t} = R \tag{2}$$

$$\nabla\cdot\vec{\mathbf{J}}_p + \frac{\partial p}{\partial t} = -R \tag{3}$$

together with:

$$\vec{\mathbf{E}} = -\nabla\psi \tag{4}$$

$$\vec{\mathbf{J}}_n = \mu_n(qn\vec{\mathbf{E}} - kT\nabla n) \tag{5}$$

$$\vec{\mathbf{J}}_p = \mu_p(qp\vec{\mathbf{E}} + kT\nabla p) \tag{6}$$

where:
q is the electronic charge,
ϵ is the permittivity,
R is the rate of recombination between electrons and holes,
μ_n and μ_p are the electron and hole mobilities,
k is Boltzmann's constant,
T is the temperature.

Note that in the preceding equations spatial vectors have been identified using an arrow symbol above the vector quantity; subsequent higher-dimensional space-time vectors will be identified using a tilde above the vector quantity.

To reformulate these equations in a space-time context we need to define a space-time gradient operator in terms of the spatial gradient and a component in the time direction specified by a unit vector, $\boldsymbol{\tau}$, i.e.

$$\square = \nabla + \frac{\partial}{\partial t}\tilde{\boldsymbol{\tau}} \tag{7}$$

Then we may re-express equations (1) to (3) as:

$$\square\cdot\tilde{\mathbf{S}}_\psi = \frac{q}{\epsilon}(D+p-n) \tag{8}$$

$$\square\cdot\tilde{\mathbf{S}}_n = R \tag{9}$$

$$\square\cdot\tilde{\mathbf{S}}_p = -R \tag{10}$$

where:

$$\tilde{\mathbf{S}}_\psi = (\vec{\mathbf{E}}, 0) \tag{11}$$

$$\tilde{\mathbf{S}}_n = (\vec{\mathbf{J}}_n, -n) \tag{12}$$

$$\tilde{\mathbf{S}}_p = (\vec{\mathbf{J}}_p, p) \tag{13}$$

The advantage of this formulation is not merely aesthetic for it allows us to achieve, for the first time, a fully conservative discretization on an effective time-varying spatial mesh using the flux vectors $\mathbf{S}_\psi$, $\mathbf{S}_n$ and $\mathbf{S}_p$. In addition a space-time viewpoint makes obvious a simple solution to the large signal problem by imposing periodic boundary conditions on the time dimension.

SPACE-TIME DISCRETIZATION

Equations (8) to (10) may be discretized in an analogous way to the steady-state form of equations (1) to (3). Consider, for example, equation (9), integrating over a volume of space-time and applying the divergence theorem, to convert the divergence term into its equivalent surface integral form, we may write:

$$\int \tilde{\mathbf{S}}_n \cdot \mathrm{d}\tilde{\mathbf{\Omega}} = \int R \, \mathrm{d}V \tag{14}$$

where $\mathrm{d}\mathbf{\Omega}$ is the outward normal to an element of the bounding surface of the space-time volume and $\mathrm{d}V$ is an elemental space-time volume. If we consider a discrete set of points in space-time and form general 'control volumes' or 'Voronoi cells' from the perpendicular bisector hyperplanes then we can replace the integral on the left of equation (14) by a summation over the faces of the Voronoi cell and assuming R is constant within the cell the right-hand side may be integrated to give:

$$\sum_{\omega} \tilde{\mathbf{S}}_{n\omega} \cdot \tilde{\mathbf{A}}_{\omega} = RV \tag{15}$$

where $\mathbf{A}_{\omega}$ is the outward normal to cell face ω and V is the space-time volume of the cell.

For any face defined by its space-time area vector we can determine spatial and temporal area components, i.e.

$$\tilde{\mathbf{A}} = \vec{\mathbf{A}}_{\mathrm{s}} + A_{\mathrm{t}} \tilde{\boldsymbol{\tau}} \tag{16}$$

equation (15) then becomes:

$$\sum_{\omega} (\vec{\mathbf{J}}_{n\omega} \cdot \vec{\mathbf{A}}_{\mathrm{s}\omega} - n_{\omega} A_{\mathrm{t}\omega}) = RV \tag{17}$$

To evaluate (17) we need to assign a value to n_{ω}, the electron concentration at the mid-point between the two nodes defining the face ω. Physically it is reasonable to express such an n as a weighted mean of the values at the two nodes:

$$n = w n_{\mathrm{pastnode}} + (1{\cdot}0 - w) n_{\mathrm{futurenode}} \tag{18}$$

For the purpose of this initial study we have chosen $w = 1{\cdot}0$ as this corresponds, on a rectangular mesh, to the backward Euler time-step method used in conventional transient analysis.

PERIODIC TEMPORAL BOUNDARY CONDITIONS

Given the above space-time discretization on a mesh that extends in the time dimension, as well as conventional space, it is possible to impose periodic temporal boundary conditions. Such boundary conditions result in a space-time topology that is cylindrical, i.e. closed in time; this forces a periodic solution with the fundamental period given by the circumference of the cylinder (Figure 1). Transients cannot exist on such a mesh and so the large signal problem can be solved by effectively integrating the governing equations over just one period of the fundamental excitation.

IMPLEMENTATION WITHIN TESSA

TESSA is written in the 'C' programming language and runs within a workstation environment. Input and output is achieved directly via our IDDE[4] graphical interface. Within TESSA topological,

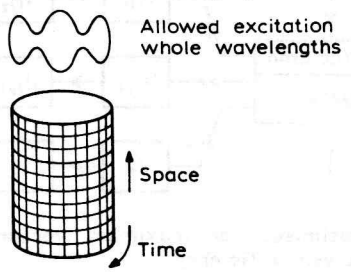


Figure 1. Periodic temporal boundary conditions

geometrical and physical data concerning a device is stored on a node-list structure, a schematic of which is shown in Figure 2. Such a structure allows periodic boundary conditions to be enforced simply by adjusting nearest-neighbour pointers within the node-list. This structure is very flexible and means that the linear solver core of TESSA can, in principle, solve any number of equations on a general Voronoi mesh in any number of dimensions provided, of course, that a description of the node-list is available and that routines to compute the matrix elements exist.

During the solution procedure a routine scans the node-list and generates a matrix appropriate to the equations being solved. A schematic of the matrix storage structure is given in Figure 3(a), which is optimized for minimum required storage space. A modification to this basic structure is shown in Figure 3(b) which maximises the solution efficiency by ensuring vector operations during LU decomposition are naturally aligned. The matrix storage structures are specifically designed for the efficient evaluation of LU decompositions to any degree of fill-in.

TESSA can employ a number of iterative techniques to solve the linear equations generated, ICCG, BI-CG, CGS and BI-CGSTAB[5] all preconditioned via incomplete LU decomposition. A direct solver based on complete LU decomposition is also provided.

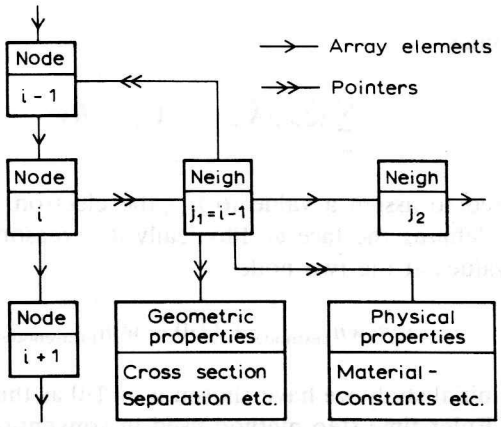
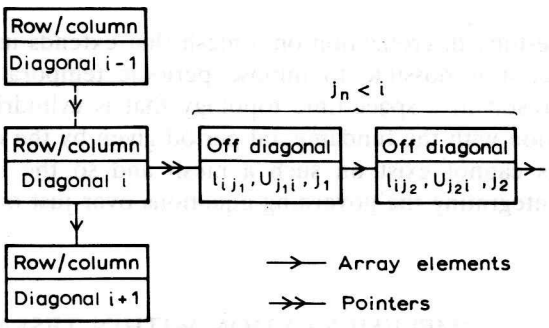
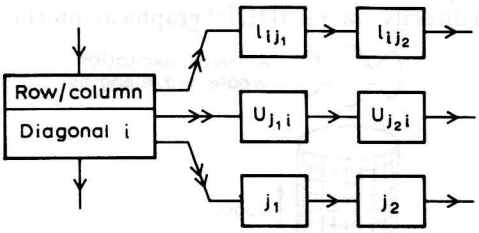


Figure 2. Schematic of node-list structure



a) Optimised for minimum storage.



b) Optimised for maximum vectorised solver efficiency.

Figure 3. Schematic of matrix structure

DIODE HARMONIC DISTORTION

To test the accuracy of the TESSA/PSS method computations of harmonic distortion were performed using TESSA for the case of a 1-D (spatial) diode, results were compared to an analytic treatment of the same case valid for small signal conditions.

Analytic modelling of harmonic diode distortion starts from the following equation for current as a function of voltage:

$$I = A(\exp(B\psi) - 1) \tag{19}$$

where I is the current whilst A and B are constants peculiar to the particular junction structure.

If ψ is of the form $\psi = \psi_{dc}+\psi_{ac}\sin(\omega t)$ then for small signal levels and low frequencies we can expand (19) as a Taylor series to obtain an expression for the amplitude, in decibels, of the nth harmonic (H_n) relative to the fundamental. This expression is itself a series expression, when evaluated to first order only we obtain:

$$H_n = 20\log\left[\frac{\left(\frac{B\psi_{ac}}{2}\right)^{n-1}}{n!}\right] \tag{20}$$

When employing a TESSA/PSS analysis the harmonic amplitudes are obtained from a Fourier analysis of the time-dependent diode current by applying the trapezoidal integration rule to obtain the Fourier amplitudes, i.e. given:

$$I(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}[a_n\cos(n\omega t) + b_n\sin(n\omega t)] \tag{21}$$

then:

$$a_0 = \frac{2}{m}\sum_{1}^{m} I_m \tag{22}$$

$$a_n = \frac{2}{m}\sum_{1}^{m} I_m\cos(n\theta_m) \tag{23}$$

$$b_n = \frac{2}{m}\sum_{1}^{m} I_m\sin(n\theta_m) \tag{24}$$

where m is the number of equally spaced time samples, I_m is the value of the diode current at the mth sample and θ_m its phase. The nth harmonic component can finally be expressed as:

$$H_n = 20\log\left[\frac{c_n}{c_1}\right] \tag{25}$$

where:

$$c_n = \sqrt{a_n^2+b_n^2} \tag{26}$$

TESSA was used to obtain, for a particular diode structure, a value for B in equation (19). This value was used in the analytic expressions for the expected distortion. Table 1 shows a comparison between the two methods under small signal low-frequency conditions for both 10 and 20 time planes in the case of TESSA/PSS. It can be seen that excellent agreement is obtained with remarkably few time planes, 10 time planes just failing to reproduce the 5th harmonic. At higher signal amplitudes, significant differences between analytic and TESSA/PSS predictions were observed, owing to the failure of the assumptions underlying the analytic approach.

Table 1. Diode distortion predictions

Harmonic	Analytic dB	TESSA/PSS dB 10 time planes	TESSA/PSS dB 20 time planes
2nd	−20·32	−20·37	−20·37
3rd	−44·16	−44·25	−44·25
4th	−70·50	−70·62	−70·62
5th	−98·78	−138·43	−98·87

TRANSISTOR DISTORTION

It is not possible to predict transistor distortion from a simple analytic expression. Therefore TESSA/PSS results must be compared with experiment.

In principle TESSA/PSS can predict multiple signal source distortions, such as intermodulation, provided all signal sources are harmonics of an underlying fundamental frequency. The number of time planes necessary to resolve all frequencies for the case of multiple signal sources may, however, be excessive and for this reason single signal source harmonic distortion is most easily predicted. Experimentally there are practical difficulties in measuring harmonic distortion as it is very difficult to separate out the distortion produced by the transistor from that generated by the signal source.

An additional problem is that, at present, external circuit elements, other than contact resistors, cannot be included within a TESSA/PSS simulation and therefore the effect of any parasitic elements or external circuitry on the distortion cannot be reproduced.

Therefore to obtain an indirect comparison with experiment a production transistor was parameterized using a standard SPICE[6] UCB model, where the parameters were optimized to give a good fit with measured intermodulation data. A harmonic balance circuit simulator LIBRA[7] was then used to predict the harmonic distortion for the 'bare' transistor as modelled by TESSA/PSS.

Figure 4 plots collector current 3rd harmonic distortion, in dB relative to the fundamental, as a function of DC collector current, the amplitude of the fundamental is held constant at 12·6 mA. Computing times were of the order of 1 hour per point on our Apollo DN10000 workstation with 8000 nodes arranged on 10 time planes. Each point required one 2-D steady-state run to initialize the DC starting condition, one small signal 3-D PSS run to obtain the AC gains, and, finally, a large signal PSS run to achieve the desired AC output power level. The circuit simulation took several minutes for the entire curve but, of course, the time taken to arrive at a satisfactory circuit model should also be considered if a fair comparison is sought.

Agreement is seen to be good up to a DC collector current of approximately 100 mA, even reproducing a cancellation at approximately 10 mA due to a 1 Ω emitter resistance included in the simulation.

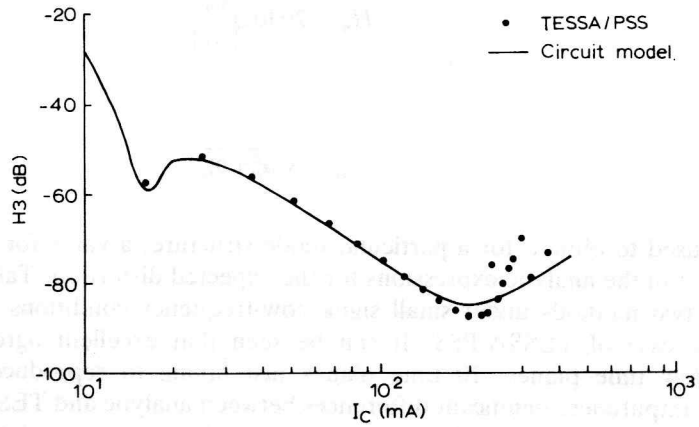


Figure 4. Third harmonic (dB) at 100 MHz fundamental

Above 100 mA a discrepancy grows, however, in this regime where velocity saturation effects are occurring, the UCB circuit model is known to be lacking in its physical content and, indeed, does not fit the experimental intermodulation data very well. An interesting feature of the TESSA/PSS results is the loss of monotonicity as distortion levels increase at very high collector currents. This could be either a real effect or a mesh-induced artefact. Figure 5 plots all the computed harmonics, up to the 5th, it can be seen that monotonicity is lost for each curve at high currents but, significantly, not at the same value of DC collector current. Note that the 5th harmonic is not well resolved on 10 time planes and can therefore be viewed as a measure of the numeric noise level.

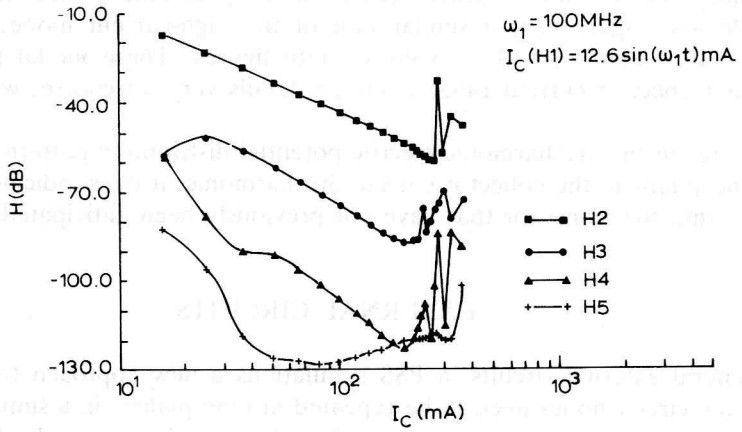


Figure 5. TESSA, transistor harmonics with V_{CE} = 5 V in a circuit with a short-circuit load and ideal voltage source

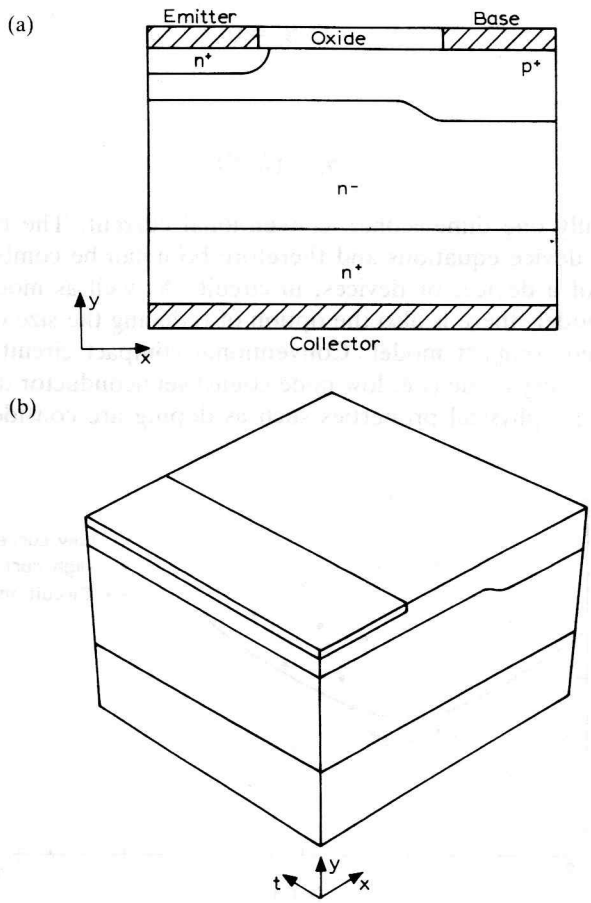


Figure 6. NPN transistor. (a) Spatial cross-section. (b) Space-time projection

For reasons explained earlier, we have no experimental data on harmonic distortion and, indeed, temperature effects that have not been included in these simulations may be important at these high current levels. We can, however, look inside the transistor, using the TESSA/PSS data, to try and determine whether the predicted high-current behaviour is real or artificial. Figure 6(a) shows the structure of the transistor under study.

TESSA/PSS-generated data on the ψ, n and p distributions can be Fourier analysed to separate out the component harmonic distributions within the device, and the results plotted on a space-time projection of the device (Figure 6(b)), in an attempt to observe where distortions are generated. It was observed that two distinct modes of the electric potential 3rd harmonic seemed to be competing for dominance in the DC current range 200 mA to 240 mA. In Figure 7 the high-current TESSA/PSS data from Figure 4 has been reproduced and the points at which the two modes exist has been indicated. Figure 8(a) shows a space-time projection of the low-current potential mode and Figure 8(b) a similar plot of the high-current mode; the contours range between $+1{\cdot}5\times10^{-7}$ and $-1{\cdot}5\times10^{-7}$ volts in both figures. These modal patterns are broadly typical of their respective current ranges, though details vary, of course, with the exact current level.

Whilst a change in the 3rd harmonic electric potential distribution pattern does not correspond exactly with the jumps in the collector current 3rd harmonic, it does indicate that processes may be occurring within the transistor that have not previously been anticipated.

EXTERNAL CIRCUITS

To include general external circuits in PSS simulations a new approach to circuit modelling is required, i.e. the circuit nodes need to be repeated in time planes, in a similar way as the device nodes are, and the current between any two nodes related to the potentials of neighbouring space-time nodes. This can be achieved by casting Kirchhoff's current conservation law into its space-time form i.e.:

$$\Box\cdot\tilde{\mathbf{S}}_c = 0 \tag{27}$$

where:

$$\tilde{\mathbf{S}}_c = (I_c, 0) \tag{28}$$

and I_c is the, essentially one dimensional, conventional current. The circuit equations are now similar in form to the device equations and therefore both can be combined to solve the general large signal problem of a device, or devices, in circuit. As well as modelling non-linear devices by detailed physical models there is also the option of reducing the size of the problem by various forms of parameterized compact model. Conventional compact circuit models are the obvious choice but, in addition, very crude (i.e. low node count) semiconductor device models are possible in which dimensions and physical properties such as doping are considered as parameters to be

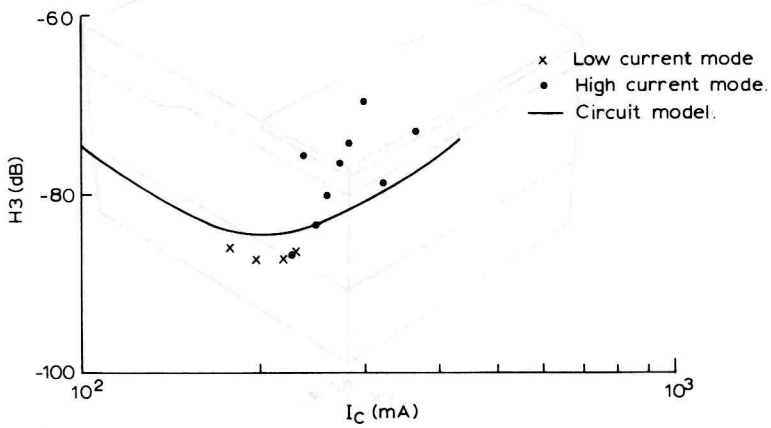
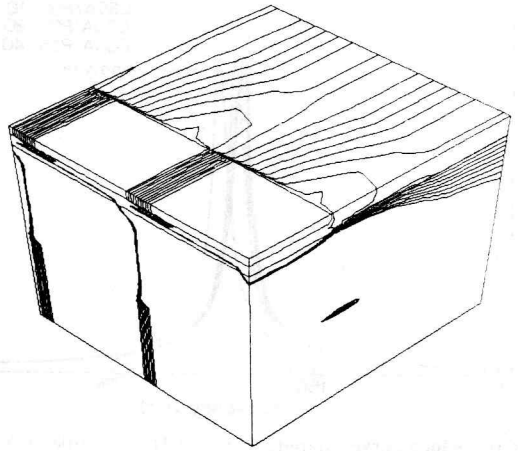
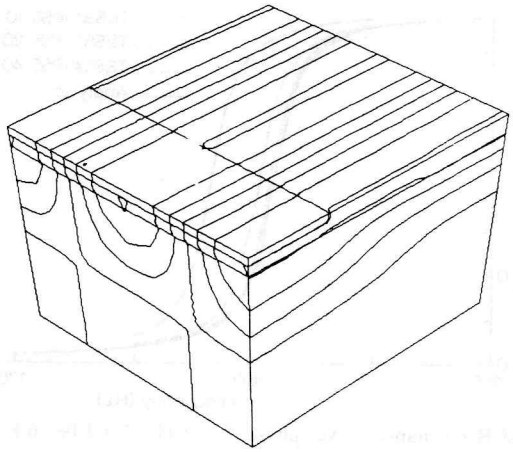


Figure 7. Third harmonic (dB) at 100 MHz fundamental



(a) Low DC current mode



(b) High DC current mode

Figure 8. Third harmonic potential distribution

adjusted to give a good fit to data. Hybrid models are also possible in which one-dimensional detailed semiconductor device models can be linked by circuit elements to represent a two- or three-dimensional device.

To test the accuracy of this approach to circuit modelling, a simple LCR series circuit was simulated under sinusoidal excitation of variable frequency. The current flowing in the individual L, C and R linear components can easily be related to the potential on neighbouring space-time circuit nodes via:

$$\mathrm{d}I = \frac{V\,\mathrm{d}t}{L} \tag{29}$$

$$I = C\frac{\mathrm{d}V}{\mathrm{d}t} \tag{30}$$

$$I = \frac{V}{R} \tag{31}$$

Figures 9(a) and (b) compare TESSA/PSS results (on 10, 20 and 40 time planes) with the analytic treatment of the LCR circuit. The agreement is seen to improve as the number of time planes increases as expected.

There are at least two ways in which the TESSA/PSS circuit approach is a simplification of the conventional numerical approach to circuit modelling. First, for each space-time node we obtain just one equation for its potential whilst the conventional method generates more equations than there are unknowns, which necessitates some work to discard excess equations before a simulation can run. Secondly, all distortion effects can be obtained after simulation by simple Fourier analysis

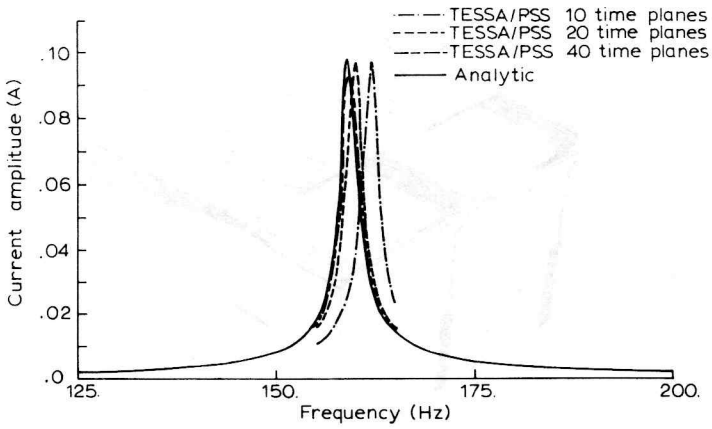


Figure 9(a). LCR resonance curve, amplitude $L = 1$ H, $C = 1{\cdot}0\mathrm{e}{-6}$ F, $R = 10\ \Omega$, $V = \sin(\omega t)$

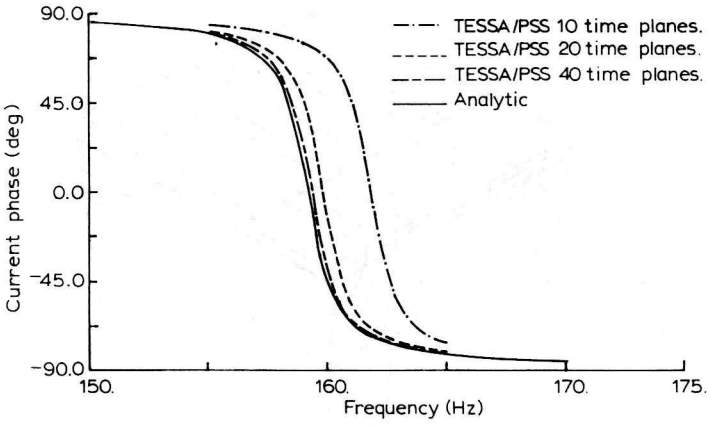


Figure 9(b). LCR resonance curve, phase $L = 1$ H, $C = 1{\cdot}0\mathrm{e}{-6}$ F, $R = 10\ \Omega$, $V = \sin(\omega t)$

without the need for deriving series expansions, as for the Volterra series approach, or for self-consistently solving the circuit equations for an *a priori* given set of harmonics, as in the harmonic balance approach.

The ability to simulate circuits and semiconductors together under large signal conditions within the same framework provides the most direct link possible between fundamental device models and compact models. Compact models are required, at present, when modelling large circuits with many non-linear elements in order to minimize simulation time but are not easily modified to accommodate device design changes. It is now possible to employ optimization techniques to parameterize a compact model in a simple circuit by reference to a fundamental device model in an exactly similar circuit within the same computer program.

CONCLUSIONS

We have, for the first time, derived a fully conservative discretization of the semiconductor device equations valid on general time-varying spatial meshes and based on a space-time formulation of the device equations.

Large signal periodic effects can be accurately and economically simulated over just one period of the excitation by imposing periodic temporal boundary conditions on a space-time mesh. Excellent agreement on predicted distortion levels is obtained between our simulations and conventional analytic/circuit modelling approaches for diodes and transistors in the regimes for which the conventional approaches are considered accurate. Significant differences are apparent outside those regimes. In addition we now have the capability to look inside a device at the sources of distortion and can therefore consider ways to minimize the effects of those sources.

It has been demonstrated that a space-time approach to circuit modelling can also be formulated so that true large signal circuit simulations can be performed and combined with device simulations.

Non-linear circuit elements may therefore be represented either by detailed physical models or by compact physical/circuit models.

It is now feasible to optimize a compact model of a device to a fundamental device model within the same computer program thus providing a direct link between device and circuit design.

ACKNOWLEDGEMENT

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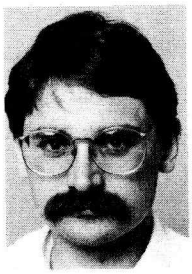
Kenneth R. Whight received the B.Sc. degree in physics from the University of East Anglia in 1972 and studied astrophysics and cosmology for one year at the University of Cambridge. He joined the integrated circuit techniques group at the Philips Research Laboratories, Redhill, in 1973 and worked on various aspects of integrated circuit research before moving to the discrete devices group, in 1978, to work on silicon power device modelling. Initially his work concerned off-state simulation, in particular the design of high-voltage junction passivation systems employing multiple floating field rings. More recently he has been concerned with the numerical and algorithmic aspects of on-state device simulation.



Paul A. Gough received the B.Sc. degree in theoretical physics from Leicester University in 1981. In the same year, he began work for Xerox Research, UK, which continued until 1982 when he joined the discrete devices group at Philips Research Laboratories, Redhill. His initial work on the transient behaviour of GTOs and transistors led to the development of a coupled circuit and device simulator HECTOR. In 1985 he was seconded to Philips Laboratories, Briarcliff Manor, New York, and became involved in the study of PICs, in particular, LIGTs. In 1986, on return to PRL, he became project leader for CAD. Inductive switching simulations of devices and the development of interactive device design software have been his recent projects. His current interests include electrothermal and 3-D device simulation.

Philip Walker received the B.Eng degree in electronics and the Ph.D. degree in semiconductor devices from Liverpool University in 1983 and 1989, respectively. From 1986 to 1987, he was a member of the academic staff in the Department of Electrical Engineering and Electronics at Liverpool University. Upon joining Philips Research Laboratories in 1987 he became a member of the Discrete Devices Group where he initially worked on computer modelling of the processing and operation of the 'intelligent power switch'. Since 1988 he has been involved in the development of generalized computer models for semiconductor device operation and processing.